AMENDMENTS TO THE CLAIMS

Without prejudice, please amend the claims as reflected in the following listing of claims, which will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method of encoding a plurality of predefined codes into a search key, the method comprising:

   a) producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predefined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said possible bit combinations; and

   b) setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes.

2. (Original) The method claimed in claim **1** wherein producing comprises arranging said bit positions in order by ascending lengths of corresponding said possible bit combinations.

3. (Original) The method claimed in claim **2** wherein producing comprises further arranging said bit positions in order by ascending numeric value of corresponding said possible bit combinations.

4. (Original) The method claimed in claim **1** further comprising producing a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet.

5. (Original) The method claimed in claim **1** wherein producing comprises producing a plurality of PNBAs, each PNBA corresponding to a sub-group of bits of said pre-defined codes.

6. (Original) The method claimed in claim **5** further comprising producing an External Subtree Root Bit Array (ESRBA) for each PNBA, said ESRBA having bit positions corresponding to possible further subgroups of bits of said pre-defined codes.

7. (Original) The method claimed in claim **6** further comprising producing a plurality of pages, each page comprising a plurality of PNBA-ESRBA pairs.

8. (Original) The method claimed in claim **6** further comprising producing a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet.

9. (Original) The method claimed in claim **8** further comprising associating with each of said PNBAs a next hop pointer pointing to a position in said next hop array at which next hop information associated with a first active bit of said PNBA is located.

10. (Original) The method claimed in claim **9** further comprising arranging said plurality of PNBAs into a plurality of respective pages, each page comprising a PNBA, an associated ESRBA, an associated next hop pointer and a next page pointer pointing to a next page in said plurality of respective pages to be searched.

11. (Previously presented) An apparatus for encoding a plurality of predefined codes into a search key, the apparatus comprising:

a) means for producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predefined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations; and

b) means for setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes.

12. (Previously presented) An apparatus for encoding a plurality of predefined codes into a search key, the apparatus comprising a processor circuit and memory in communication with the processor circuit, said memory being configured to direct the processor circuit to:

a) produce a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predefined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations, and

b) set bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes.

13. (Currently amended) The apparatus claimed in claim **12** wherein said memory ~~processor~~ is configured to direct said processor circuit to arrange said bit positions in order by ascending lengths of corresponding said possible bit combinations.

14. (Currently amended) The apparatus claimed in claim **13** wherein said memory ~~processor~~ is configured to direct said processor circuit to further arrange said bit positions in order by ascending numeric value of corresponding said possible bit combinations.

15. (Currently amended) The apparatus claimed in claim **12** wherein said memory ~~processor~~ is configured to direct said processor circuit to produce a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet.

16. (Currently amended) The apparatus claimed in claim **12** wherein said memory ~~processor~~ is configured to direct said processor circuit to produce a plurality of PNBAs, each PNBA corresponding to a sub-group of bits of said pre-defined codes.

17. (Currently amended) The apparatus claimed in claim **16** wherein said memory ~~processor~~ is configured to direct said processor circuit to produce an External Subtree Root Bit Array (ESRBA) for each PNBA, said ESRBA having bit positions corresponding to possible further subgroups of bits of said pre-defined codes.

18. (Currently amended) The apparatus claimed in claim **17** wherein said memory ~~processor~~ is configured to direct said processor circuit to produce a plurality of pages, each page comprising a plurality of PNBA-ESRBA pairs.

19. (Currently amended) The apparatus claimed in claim **17** wherein said memory ~~processor~~ is configured to direct said processor circuit to produce a next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet.

20. (Currently amended) The apparatus claimed in claim **19** wherein said memory ~~processor~~ is configured to direct said processor circuit to associate with each of said PNBAs a next hop pointer pointing to a position in said next hop array at which next hop information associated with a first active bit of said PNBA is located.

21. (Currently amended) The apparatus claimed in claim **20** wherein said memory ~~processor~~ is configured to direct said processor circuit to arrange said plurality of PNBAs into a plurality of respective pages, each page comprising a PNBA, an associated ESRBA, an associated next hop pointer and a next page pointer pointing to a next page in said plurality of respective pages to be searched.

22.-70. (Canceled)

71. (Previously presented) A computer readable medium encoded with codes for directing a processor circuit to carry out the steps recited in claim **1**.

72. (Previously presented) A computer readable signal encoded with codes for directing a processor circuit to carry out the steps recited in claim 1.